



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/900,940	07/09/2001	David N. Pether	00-339 1496.00116	9547

24319 7590 08/11/2004  
LSI LOGIC CORPORATION  
1621 BARBER LANE  
MS: D-106 LEGAL  
MILPITAS, CA 95035

EXAMINER

KOSTAK, VICTOR R

ART UNIT PAPER NUMBER

2614

DATE MAILED: 08/11/2004

4

Please find below and/or attached an Office communication concerning this application or proceeding.

h

**Office Action Summary**

Application No.

09/900,940

Applicant(s)

PETHER, DAVID N.

Examiner

Victor R. Kostak

Art Unit

2614

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 24 May 2004.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

Art Unit: 2614

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the memory now recited in claims 1 and 12 (which is purportedly a key element and is not the memory 114 shown) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. Applicant's arguments filed on 05/24/04, in view of the amendment, have been fully considered but they are not persuasive, explained as follows.

Applicant first argues that his system is distinct from Bilbrey by saying that the title describing Bilbrey "contrasts" with applicant's disclosing of a first and a second circuit (page 8

Art Unit: 2614

of the response). That is specious logic. One of ordinary skill in the art does not refer to a broadly phrased title to encompass the entirety of the patent disclosure.

Moreover, believing that Bilbrey does not disclose first and second circuitry is as erroneous. Bilbrey clearly discloses first, second, third, and a multitude of circuitry, and other components within those circuitry that are *themselves* plural respective circuitry. The computer on which the examiner drafted this communication - as well as the associated printer from which this communication was produced – have first and second circuitry, as well as third, fourth, fifth, and so on, to some large amount of circuitry completing their systems.

Applicant is also incorrect when he alleges that the three inputs to component 68 do not and cannot comprise pixels because (first) these signals are “*consistently described*” as “*the three analog signals*”, and (second) that “*one skilled in the art would understand that analog signals do not comprise a plurality of input pixels*” (page 9 of the remarks).

In the first place, Bilbrey introduces these analog signals as “*video*” signals (col. 4 line 66). Bilbrey does not have to continuously spell out their entire designation just as applicant apparently chose not to spell out “*alpha multiplier and accumulator*” since he refers to that element as a “*MAC*” thereafter. Secondly, analog signals can very easily comprise pixels as explicitly disclosed by Banker (col. 12 lines 47-54).

Fact is, fundamentally and technically speaking, pixels are not signals that are in transition for storing, transferring or processing. “Picture elements” are actual pixels when initially captured by a scanner individually identified per respective X - Y positions on a sensor, or when ultimately presented on a display per respective X – Y positions on the screen. The storing, transferring and processing involves *signals representing* the pixels – not any actual

Art Unit: 2614

pixels. It is understood that describing pixel processing in fact involves processing of signals representing those pixels. The convenience of minimizing superfluous language unnecessary to the understanding of actual processes has arisen and has been broadly accepted, evident in Banker, for example. The examiner could have raised issues of misdescriptiveness regarding applicant's "pixel processing" otherwise.

Regarding another point, applicant's rhetorical question regarding *new* claim 22 (page 10 of the remarks) is not appropriate since the examiner has yet to have seen that new claim.

In view of these arguments countering applicant's, the rejection claims 13-21 accordingly stands as applied in the last Office action, repeated below to consolidate the issues. The feature of "pixel processing" has been addressed above. The feature of allowing one or more input pixels to contribute to the creation of one or more output pixels is addressed in the context of claim 13 below.

Applicant's amended claims 1-12 and 22 have now been rejected using other art, due to the explicit recitation of the memory and its usage.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 13-21 stand rejected, as amended, under 35 U.S.C. 102(b) as being anticipated by Bilbrey et al.

Art Unit: 2614

Reviewing Bilbrey, his multiple effect video processing system, Bilbrey presents comprehensive disclosure of hardware and functionality of the hardware components used to alter resolution, for example (by moasicking, for example: col. 47 line 32+). The arrangement of blocks 20, 30 and 40 can be considered a first (composite) circuit that generates a signal having a first resolution for eventual display on monitor 42, derived from an input signal having a second resolution according to control signals, and the microcomputer 50 can be considered the second circuit which generates the control signals (used to generate the first signal from the second) in response to a previous calculation by the first circuit and various input parameters (e.g. pixel intensities, color values, horizontal and vertical image dimensions, etc.), wherein the microcomputer directs the second circuit to scale and filter the input signal (e.g. col. 1 lines 21-32, filtering carried out by pixel dropping and range thresholding, for example). The controller is initially informed of the input signal parameter calculations from the first circuit in order to know what exact parameters must be used for converting it into the second signals.

Alternatively, the claimed first circuit can read on the arrangement of elements 30, 40 and parts of element 20, and the second circuit (used for control signal generation and application) can read on the microcomputer 24 associated with interface controller 24, which components together carry out the selected effect processing according to programmed and adjusted control signals.

The output video signal (pixels) is based directly on the signal values of the input signal (pixels) on which conversion processing is performed to generate the output signal, thereby meeting claim 13. Generally speaking, scaling, blending, or any other conversion processing of

Art Unit: 2614

pixel data to transform it (which Bilbrey does) inherently involves the output pixels being a function of, or derived from, the input pixels.

As for claim 14, three-component video signals are manipulated (e.g. RGB shown as composite element 68 in Fig. 1).

As for claim 15, alpha data is also used with the three-color video data for manipulation (e.g. output element 36 in Fig. 16).

Regarding claim 16, the horizontal and vertical image dimensions are operated on separately (e.g. col. 47 line 32+).

Considering claim 17, the cells (or blocks) are operated on in the effect processing (noting again col. 80 line 31+).

As for claim 18, the cells are read on a line-by-line basis (reviewing again col. 80 line 31+).

As for claim 19, the lines are process a line, write it into memory, and process the next line on a continuous basis (Bilbrey includes plural various memories including at least video buffer 56 shown in Fig. 1).

Regarding claim 20, Bilbrey discusses filtering throughout his disclosure (including both spatial and temporal), and in col. 15 spanning lines 21-68, filtering is discussed as a function applied to various effect processing (including mosaicking or scaling) for further effecting image appearance.

As for claim 21, multiple input signals can be simultaneously applied for blending, for example (e.g. col. 16 line 57+).

4. Claims 1-3, 5, 10, 11 and 22 are now rejected under 35 U.S.C. 102(b) as being anticipated by Chen et al.

The system of Chen (noting particularly Figs. 1-3, 6 and 9) includes a first circuit comprising DRAM 308 (which contains both pixel data and processing commands: section 301) calculates and writes a signal having a first resolution and plural pixel data into the memory portion of the DRAM in response an input signal having a second resolution comprising plural pixels read from the memory with associated control signals (carried out by blitter (block-move) engine 906; and a second circuit ASIC 200 used to generate the control signals in response to the DRAM commands (i.e. the first circuit) and to (at least) one input parameter such as scaling factor (additionally noting host CPU 303 in Fig. 3), which results in the input signal to be scaled and filtered (i.e. alpha blended), and which conversion involves the input pixels as contributing to the output pixels of the converted signal (e.g. col. 4 lines 8-22; col. 5 lines 38-50; col. 6 lines 57-61; col. 7 lines 58-65), thereby meeting claims 1 and 12.

As for claims 2 and 3, the input signal can comprise color components with an alpha blend value (e.g. RGB: col. 7 lines 60-63).

As for claim 5, the system can include a block-move engine (i.e. blitter engine) 203, 304, 906, mentioned above.

Regarding claim 6 the system is arranged and intended to operate on multiple blocks (noting the operation of Fig. 9, for example).

As for claims 10 and 11, the system operates on the pixel data of the input signal to generate the converted output signal (in a scaled and/or alpha-blended format).

Considering claim 22, a CPU 303 is connected to the second circuit by way of a bus 305/307.

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. in view of Bilbrey et al.

Chen discloses scaling (e.g. col. 5 lines 47-48; col. 6 lines 57-61) which inherently involves altering the dimensions in both the horizontal and vertical directions, but does not provide specific details.

It would have been obvious to convert the first dimension and then the second as taught by Bilbrey (e.g. col. 47 line 32+) to complete the scaling for the clear purpose of providing the second dimension with already converted data, and for dedicating specific processing per operation.

6. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al.

Since Chen incorporates a blitter engine, which inherently move blocks of data at a time, it would have been obvious to any group of data that is a factor of the whole image frame, such as a line (; Fig. 6 depicts various sections for special effects; Fig. 9 depicts whole frames).

Art Unit: 2614

The writing back into the memory (as shown in Fig. 9) would accordingly be carried out per line to complete the entirety of the frame conversion.

7. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. in view of Watson et al.

It would also have been obvious to manipulate the data as so preferred (suggested by Chen in general terms by including special effects), such as by filtering data (besides the blending filtering), in order to further alter the image to achieve any desirable effect, such as to enhance the image as taught by Watson (col. 6 lines 41-48), who also incorporates a blitter engine 322.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant should make particular note of Watson, Cook, Chapple, and MacInness. They all disclose blitter engines and special effects (e.g. alpha blending), controlled by a CPU or another type of controller, and include multiple circuitry.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

Art Unit: 2614

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor R. Kostak whose telephone number is 703 305-4374. The examiner can normally be reached on Monday - Friday from 6:30am-3:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John W. Miller can be reached on 703 305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

**Any response to this final action should be mailed to:**

Box AF  
Commissioner of Patents and Trademarks  
Washington, D.C. 20231

**Or faxed to:**

Art Unit: 2614

**(703) 872-9306 (for Technology Center 2600 only)**

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 308-HELP.



Victor R. Kostak  
Primary Examiner  
Art Unit 2614

VRK